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For practical use of microwave simulations in industry applications such as high frequency product design, this paper presents a conceptual design of 3D FDTD dedicated computer with dataflow architecture as one of portable high performance computing technologies. A basic concept of the dataflow architecture for the FDTD dedicated computer itself was presented already in 2003 for two-dimensional microwave simulations. Detail design of 3D FDTD dataflow machine is considered in this paper.

***Index Terms*— Microwave simulation, FDTD method, Dedicated computer, FPGA, High performance computation.**

I. Introduction

Although there has been remarkable progress of a high performance computer technology in the last decay, the computer performance is still insufficient in industry applications of electromagnetic field simulations. The electromagnetic field simulations are frequently used for product design in industry. In that case, the computer platform of the numerical simulation is often prepared accompanying with a design software such as the CAD installed in a standard PC, and therefore electromagnetic field simulations are not always carried out on high-end computers. In addition, the electromagnetic field simulations themselves require us very long computation time even if the highest-end computers such as supercomputers or GPU clusters are employed when very large numerical models of order of over 1,000 x 1,000 x 1,000 grid space are simulated. Accordingly, for effective use of the electromagnetic field simulations in industry, it is required to prepare any "portable high performance computation" technologies which operate accompanying with standard PCs for the CAD.

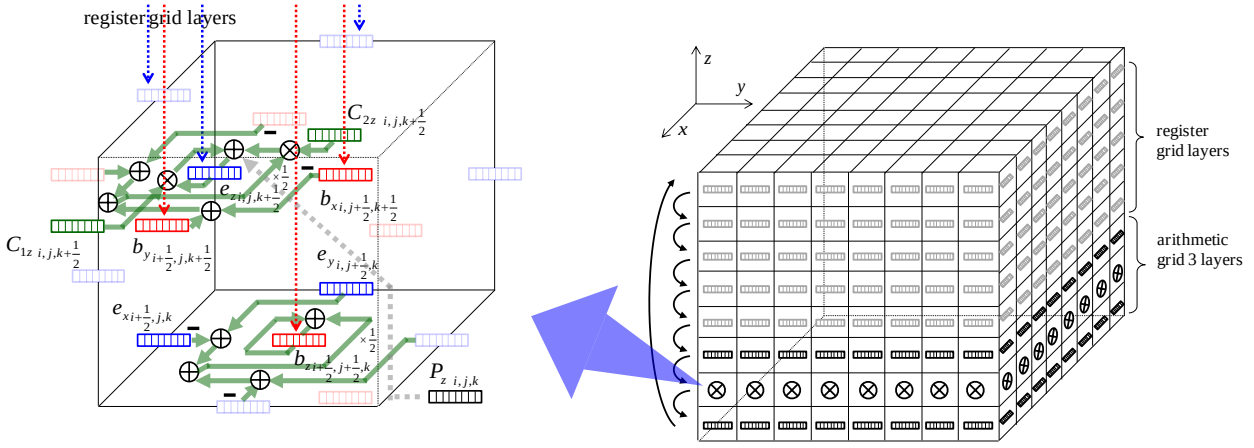
As one of solutions to such requirements of the portable HPC in a field of microwave simulations, a method of dedicated computer of the FDTD method was presented [1]-[9]. To construct hardware circuits and memory access architecture optimizing to the FDTD scheme by using a reconfigurable LSI such as the FPGA, high performance computation machines can be utilized by much smaller size and lower cost than the supercomputers or GPU clusters. Actually various kinds of hardware architectures of the FDTD scheme were proposed and installed in real hardware such as the FPGA, and it was shown that the designed hardware operated normally. However, all of such the FDTD dedicated hardware could not achieve sufficiently higher performance operation than the high-end PCs or the GPU computers. [9] In the FDTD dedicated computers, the FDTD scheme and memory access themselves were efficiently executed by the dedicated hardware architecture, but the clock frequency of the FPGA was too slow speed compared with PCs and GPU, which was less than 100 MHz. In those FDTD dedicated computers, the FDTD calculations are done basically grid by grid, which is intrinsically same procedure as software processing as in the PCs and GPU computers.

Accordingly we need to adopt much higher architecture of the FDTD dedicated computers to employ parallel properties hidden in the FDTD scheme for achievement of the potable HPC, which can be practically used in industry. As one of possibility of such extremely high performance computation, a dataflow architecture FDTD machine was proposed [10]. But the dataflow architecture was designed only for two-dimensional FDTD method owing to limited circuit size of those days FPGA. In this paper, beyond on recent remarkable progress of LSI technologies, a conceptual design of three-dimensional FDTD method dedicated computer with the dataflow architecture is presented to aim to extremely high performance computation for microwave simulations.

II. Dataflow architecture FDTD dedicated computer

The dataflow architecture for the FDTD dedicated computer itself was proposed for 2D microwave simulations in 2003[10]. However, hardware size and I/O pins of the FPGA were insufficient for 3D FDTD machine in those days. According to recent remarkable progress of FPGA technologies, we here present a detail design of 3D FDTD dataflow machine.

Figure 1 shows a configuration of 3D FDTD dedicated computer with dataflow architecture. Data registers are allocated in 3D grid space in same manner as electromagnetic field components of Yee's grid, and then registers in the lowest layer are connected each other by digital circuits which execute the FDTD scheme of three components in a single clock. (see Fig.1(a)) After the execution of circuit operation of the FDTD scheme, register data in all region are shifted down in cyclic manner by one layer. (see Fig.1(b)) To repeat this process for all vertical layers for both electric and magnetic fields, one time step FDTD calculation for the entire grid space is executed by 4 x Z clock cycles (Z is the number of vertical layers). In this architecture, there are no memory accesses which are biggest overhead in the Neumann's architecture machines, and its performance is purely proportional to the number of grids in horizontal plane and system clock frequency.



(a) digital circuit of FDTD scheme on arithmetic layer (b) entire grid structure of FDTD machine

Fig.1 Configuration of 3D FDTD dedicated computer with dataflow architecture

III. Detail Specification of FDTD Dataflow Machine for Practical Simulation

One of most important tasks in the development of the dedicated hardware is flexibility for various situations of simulations. For example, it is necessary to design the hardware to be commonly used for various numerical models including complicated 3D shapes and any distributions of material constant without any modifications of the machine hardware. In addition, flexible allocation of absorbing boundary condition (ABC) should be available without any hardware modifications. To satisfy these conditions, we need to construct the digital circuit to be operated as both modes of normal and a perfectly matched layer (PML) grids. One more requirement for the dataflow architecture machine is reduction of the hardware size because this architecture leads to huge hardware size compared with other conventional architectures.

We here use the following Maxwell's equations to be applied to most general cases including the PML grids,

$$\nabla\times\mathbf{E} = -\sigma^{*}\mathbf{H} - \mu\frac{\partial\mathbf{H}}{\partial t} \quad . \qquad (1)$$
$$\nabla\times\mathbf{H} = \sigma\mathbf{E} + \varepsilon\frac{\partial\mathbf{E}}{\partial t} + \mathbf{J}$$

To introduce the following modified unknowns,

$$\mathbf{e} = \frac{\mathbf{E}}{c_0},\ \mathbf{b} = \mathbf{B},\ Z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} = c_0\mu_0 \qquad (2)$$

we obtain the following normalized Maxwell's equations,

$$\nabla\times\mathbf{e} = -\frac{\sigma^{*}}{Z_0\mu_r}\mathbf{b} - \frac{\partial\mathbf{b}}{c_0\partial t} \qquad (3)$$
$$\nabla\times\mathbf{b} = Z_0\mu_r\sigma\mathbf{e} + \varepsilon_r\mu_r\frac{\partial\mathbf{e}}{c_0\partial t} + \mu_r\mu_0\mathbf{J}$$

where c_0, ε_0, μ_0, ε_r, μ_r are the velocity of light, permittivity, permeability in vacuum, relative permittivity and relative permeability, respectively. And, descretization of (3) on the grid space yields the FDTD formulation for the dedicated computer. For example, e_z component of the FDTD formulation is as follows,

$$e_{z\,i,j,k+\frac{1}{2}}^{n+1} = C_{z1}e_{z\,i,j,k+\frac{1}{2}}^{n+1} - p_{z\,i,j,k+\frac{1}{2}}^{n+\frac{1}{2}} + \frac{C_{z2}}{2}\left[b_{y\,i+\frac{1}{2},j,k+\frac{1}{2}}^{n+\frac{1}{2}} - b_{y\,i-\frac{1}{2},j,k+\frac{1}{2}}^{n+\frac{1}{2}} - b_{x\,i,j+\frac{1}{2},k+\frac{1}{2}}^{n+\frac{1}{2}} + b_{x\,i,j-\frac{1}{2},k+\frac{1}{2}}^{n+\frac{1}{2}}\right] \qquad (4)$$

where

$$C_{z1} = \frac{2\varepsilon_{r\,z} - c_0\Delta t Z_0\sigma_z}{2\varepsilon_{r\,z} + c_0\Delta t Z_0\sigma_z},\quad C_{z2} = \frac{2}{2\varepsilon_{r\,z}\mu_{r\,z} + c_0\Delta t Z_0\mu_{r\,z}\sigma_z}, \qquad (5)$$

p_z is a power input signal and ε_{rz}, μ_{rz}, σ_{rz} are relative permittivity, relative permeability and conductivity for e_z, respectively. Courant's condition is invoked in (4) as $c_0\Delta t = \Delta l/2$. In the same manner, for e_z at the PML grids,

$$e_{zx\,i,j,k+\frac{1}{2}}^{n+1} = C_{x1}e_{zx\,i,j,k+\frac{1}{2}}^{n} + \frac{C_{x2}}{2}\left[b_{y\,i+\frac{1}{2},j,k+\frac{1}{2}}^{n+\frac{1}{2}} - b_{y\,i-\frac{1}{2},j,k+\frac{1}{2}}^{n+\frac{1}{2}}\right] \qquad (6)$$
$$e_{zy\,i,j,k+\frac{1}{2}}^{n+1} = C_{y1}e_{zy\,i,j,k+\frac{1}{2}}^{n} - \frac{C_{y2}}{2}\left[b_{x\,i,j+\frac{1}{2},k+\frac{1}{2}}^{n+\frac{1}{2}} - b_{x\,i,j-\frac{1}{2},k+\frac{1}{2}}^{n+\frac{1}{2}}\right]$$

It is notified that all the terms in (4) and (5) have same order values each other by the normalization (2) since C_{z1}, C_{z2} are smaller than unity owing to the definition (5). This implies that we can avoid to use standard floating point expression for binary numbers and calculate (4) and (5) by using fixed point expressions, which are stored by much smaller size hardware compared with the floating point expressions (4 Bytes for single precision, 8 Byte for double precision). Accordingly the digital circuit size can be reduced effectively.

To achieve the flexible operation in the FDTD dedicated computer, the detail circuit of the arithmetic grids of Fig.1(a) are designed as in Fig.2. Initial field values e_x, e_y, e_z, b_x, b_y, b_z, material constants C_{x1}, C_{x2}, C_{y1}, C_{y2}, C_{z1}, C_{z2}, and two 1-bit information of "normal/PML" and "PEC/vacuum" for all 3D grids are downloaded from the host PC to the FDTD machine in advance of the calculation operation. To specify these download information appropriately depending on each grid, the circuit of Fig.2 automatically executes (4) or (6). That is, when 1-bit information of "PEC/vacuum" is '0', the final result of the circuit is being clear, which means the corresponding grid is a perfect electric conductor. For "PEC/vacuum" is '1' which corresponds to a vacuum or material grid, the final result of the circuit is set into the register. And if 1-bit

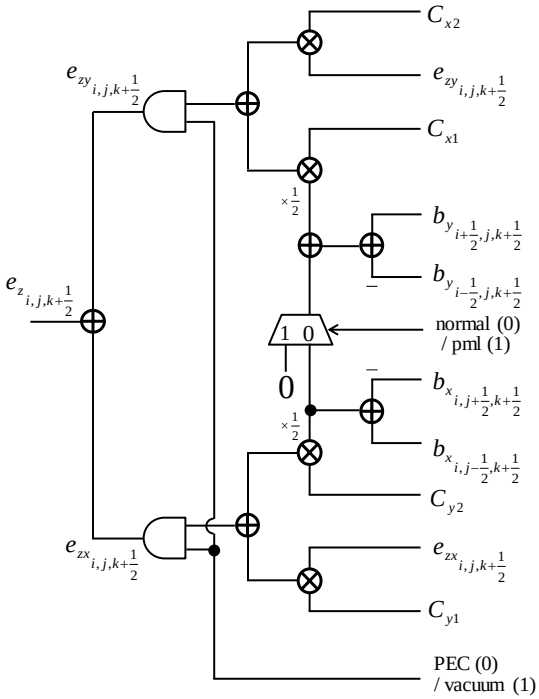


Fig.2 FDTD dual mode circuit for normal and PML grid

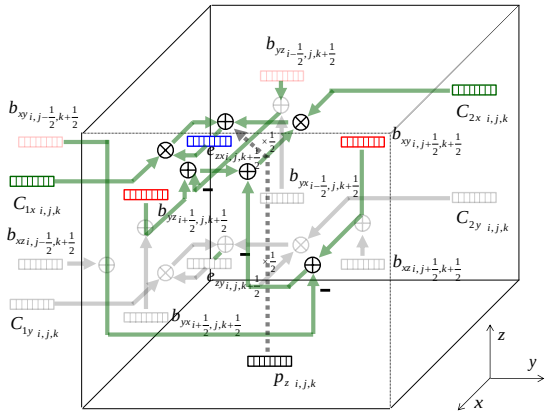
information of "normal/PML" is set to be "0", the circuit of Fig.2 executes (4), otherwise the circuit executes (6). A conceptual operations of the normal (a) and PML (b) grids on the same hardware circuit are indicated in Fig.3. Accordingly the FDTD dataflow machine automatically simulates microwave phenomena for any shapes of the PEC scatterers and any material constant distributions including the PML absorbing boundary condition by specifying appropriate download information by the host PC, without any modification of the hardware circuit.

IV. Module Structure of FDTD Dataflow Machine

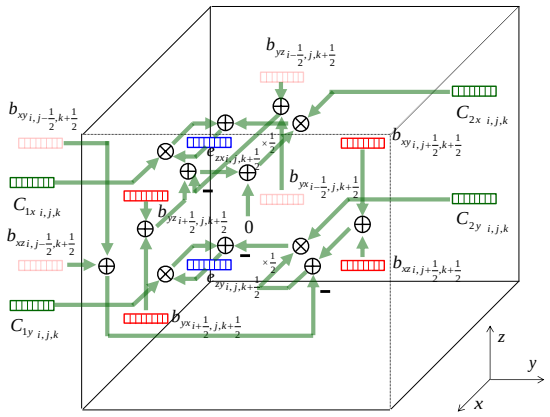
3D FDTD dataflow machine was designed by a hardware description language, the VHDL. For flexibility in construction of the FDTD grid space, the VHDL program has hierarchy structure indicated in Fig.4. The arithmetic grid layers, which are located at the lowest level in 3D grid space, consist of three layers, since the FDTD calculation needs to use one neighbor grids for all directions, therefore, upper and lower grids should be closely connected with the FDTD calculation circuit. (see Fig.4(a)) The upper layers beyond the arithmetic three layers include set of registers (Fig.4(b)) in which field values, material constants and two 1-bit information of the grid properties are stored and vertically shifted down. To combine these circuit grids, an array of a unit vertical grid is constructed as in Fig.4(c), and the entire machine of Fig.1(b) is build-up to horizontally connect this unit vertical gird array both for *x* and *y* directions.

V. Numerical Examples

The circuit of 3D FDTD dataflow machine designed by the VHDL was tested by the numerical example of a rectangular waveguide including a metal tuning screw and a metal block



(a) normal grid mode (normal/PML = '0')



(b) PML grid mode (normal/PML = '1')

Fig.3 FDTD circuit operation for normal and PML grids

(Fig.5). The entire grid space is defined by 12 x 7 x 40 size for *x*, *y*, *z* direction, respectively. Then the PML (4 layers) is allocated at both edges in *z* direction, and other outer boundaries are assumed to be PEC. The power input is imposed on *x*-y plane at 10th grid distance from the PML as continuous TE10 mode signal of E_y component. The numerical model is simple and small size, but it is sufficient to confirm normal operation of the designed circuit of the FDTD dedicated computer since all functions of the dedicated computer are invoked in this numerical model.

The figures 6 show distributions of amplitude of electric field on a middle vertical plane (see Fig.5) at 63th time step, which are calculated by C software simulation (Fig.6(a)) and virtual operation of the FDTD dataflow machine by the VHDL logic simulation (Fig.6(b)). In the VHDL design of the FDTD dataflow machine, all field values are stored by the fixed point expression in 16-bit registers. We find good agreement in Fig.6 although such the low resolution data format of 16-bit is employed, and can confirm that the designed circuit will operate normally by the good agreement. If we assume that the FDTD machine operates in 50M Hz clock, the machine performance is estimated as 1G cell/sec, which exceeds a typical performance of a single GPU, 240 M cell/sec [9].

VI. Summary

In this paper, the dataflow architecture dedicated computer

of 3D FDTD scheme has been presented to aim the portable HPC of microwave simulations. It has been shown that efficient processing of the FDTD scheme can be achieved to fully use parallel properties hidden in the FDTD scheme and remove memory access architecture. The proposed architecture of 3D dataflow architecture machine of the FDTD scheme was designed by the VHDL and its normal operation was confirmed by logic simulations.

To use small size FPGA, the hardware size of a single three arithmetic grid (Fig.4(a)) is roughly estimated as 3,300 logic elements (LE). For example, it is estimated that the highest-end FPGA with 4M LE can construct 32 x 32 *x*-*y* gird space at least, and this means that its performance will be about 12 G cell/sec, which is 50 times higher than that of the typical GPU performance. For practical applications, more complicated and larger size numerical models have to be simulated. For such tasks, further efforts of reduction of hardware circuit size and consideration of parallel computation system will be done in near future.

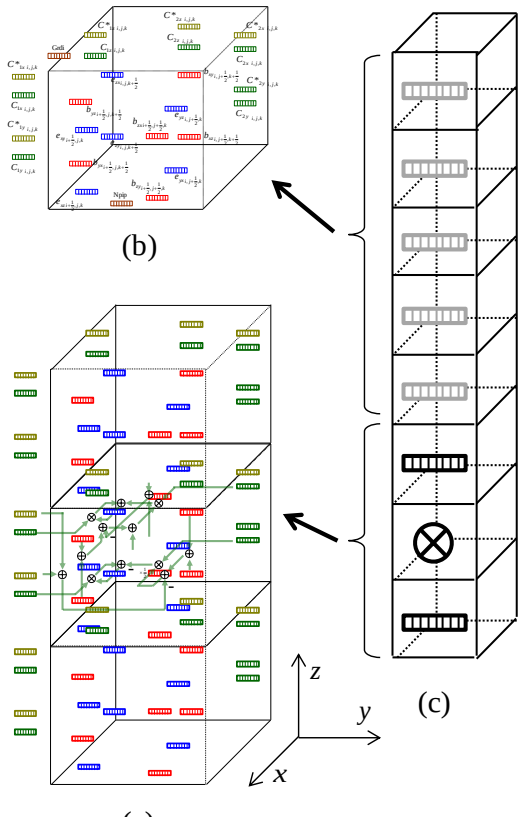


Fig.4 Module structure of FDTD dataflow machine
(a) unit arithmetic three-grids, (b) unit register grid,
(c) unit vertical grids array of FDTD dataflow machine

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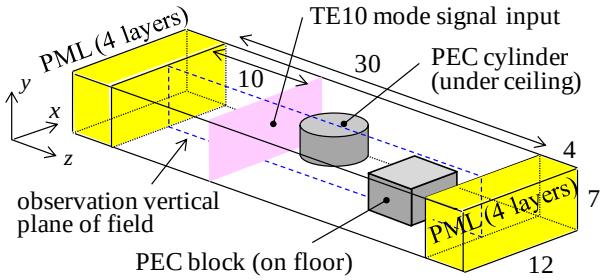
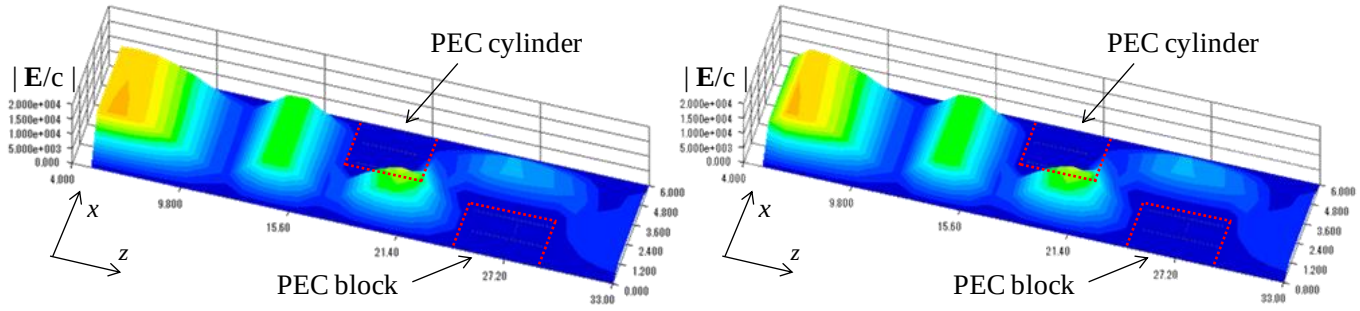


Fig.5 Numerical model of rectangular wave guide



(a) software simulation by C (b) VHDL logic simulation of FDTD machine operation

Fig.6 Electric field distributions in middle horizontal plane at 65th time step