Anodic Oxidation of Narrow Region of Silicon Substrate

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Abstract

Anodic oxide films were formed on comparatively small area of silicon substrates. Constant current mode of anodization has been used for oxidation, but during oxidation processes, the current density has been changed to go through one or more stepped transitions either step-up or step-down before the completion of the processes. This modified mode of constant current anodization showed to be effective in reducing the interface state density of a silicon/silicon-oxide system.

Among the various stepped transitions in the modified mode of constant current anodization, step-down transition of current density was found to be optimum in reducing the interface-state density. The structure and composition of SiO_2/Si interface regions for both large-area oxide and narrow-area oxide were also investigated by X-ray photoelectron spectroscopy (XPS). The composition of SiO_2/Si interface of narrow-area oxide showed less stoichiometry than that of large-area oxide.

1 INTRODUCTION

The characteristics of commercially available Si devices are very affected by the quality of oxide. To make a good quality oxide, several methods of oxide formation techniques have been developed in the past years. They are vapor phase reaction[1], plasma anodization[2], wet electrochemical anodization[3], and thermal oxidation in both dry and wet oxygen environments[4]. Among these techniques, thermal oxidation process is the most commonly used technique and the key process to grow silicon dioxide layer, but the development of the other processes of oxidation equally acceptable and applicable has been still in progress.

Anodic oxidation often termed as anodization, is one of those processes of which the detailed mechanism is not well understood at present time. In anodic oxidation, there are two types of process which are the oxidation of the surface of silicon electrode in a liquid

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electrolyte and in gaseous plasma. The major advantages[5] of anodically grown oxide films of silicon are : since the anodization is carried out at room temperature there is no impurity redistribution at the silicon surface as there is in thermal oxidation, the implementation of the equipment for oxidation process is easy and low in cost and the oxide thickness control is very precise. Conventional system for forming thermal SiO_2 is complicate and expensive compared to anodic oxidation system.

With the progress of compound semiconductor IC's and amorphous semiconductor electronic devices, oxide films grown at low temperature have been in demand recently[6]. For integrated circuits using MOS field effect transistor (MOSFET) as the active element, the behavior of some charges in the MOS system have caused the new important problems. From the point of view of realistic manufacturing conditions, acceptable densities of above mentioned charges are of the order of 10^{10} charges/cm^2 [7]. To analyze the electrical properties of a Si-SiO_2 systems, it needs to know precisely that the various charges and traps present in the oxide as well as in Si-SiO_2 interfacial region. There are four basic types of traps and charges : mobile Ionic charge (Q_m), fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}) and interface trapped charge (Q_{it}). Interface trap charge (Q_{it}[7]), which are charges located at the Si-SiO_2 interface with energy states in the silicon-forbidden bandgap, can exchange charges with silicon. If these states are not exist in near interfacial region, the Si device characteristics approach to their ideal ones.

As in thermal oxide, the interface states in anodically grown silicon oxide are relevant to the inherent electrical active centers which originate from a variety of effects and treatments in fabrication processes. Since anodic oxidation is performed at room temperature the effect of oxidation temperature is negligible. Whereas for the case of thermal oxidation it acts as a dominant factor in creating the so called detrimental traps. In anodic oxidation, the different interface states due to the contaminations incorporated and having energy state in silicon forbidden band from in thermal oxidation may appear. Precise knowledge of and researches on anodic oxidation mechanism are still insufficient but this anodic oxide growing process has certain advantages over that of widely accepted thermal grown technique.

The purpose of this study is to grow oxide films suitable for fabricating miniature MOS type devices, and the main attention is provided to grow and probe some of considerably small-dimensional oxide films. The structure and composition of SiO_2/Si interface regions for both large-area oxide and narrow-area oxide were comparatively investigated by X-ray photoelectron spectroscopy (XPS). Through a recently done work[8] we have come up with

the result that for a small-dimensional oxide, interface state density N_{it}, derceases with increasing the current density of anodization.

The constant current mode anodic oxidation was carried out to set experimental parameters to be optimum in reducing N_{it} for small-dimensional oxide formation. For a large sized anodic oxide formation, however, the effect of changing the current density exhibit an inverse relationsship between current density and N_{it} with respect to that for a small-dimensional oxide formation. The term small-dimension is used to refer a Si substrate which had a surface area in the millimeter square ($<1\ mm^2$) range. The formation of anodic oxide on narrow-area silicon substrate has been done through window to be opened in the thermal oxide by photolithographic technique.

2 EXPERIMENTAL

Boron doped, prepolished p-type (111) Si wafers with resistivity of 10～20 or 25～50Ω-cm were used. Average resistivity of the Si wafer was measured by using the four-point probe technique[9]. The Si wafer was cut into 1.5 by 1.5 cm square chips and the chips were rinsed in deionized water, in methyl alcohol and in trichlroethylene solution prior to acid etching[8]. The etching treatment has been done to make the surface of the samples flat and in mirror-like. The samples were also immersed in aqua regia to make in surface free from metal contamination. The samples were finally submerged in diluted hydrofluoric acid (DHF) just before placing them in thermal oxidation furnace.

Wet thermal oxidation was adopted in growing the field oxide. The field oxide acts as a mask during the anodization of the small area Si substrates. Thermal oxidation was carried out in a atmosphere constituted with a combination of water vapor and oxygen. It was a constant temperature process and the temperature was kept at 1060 °C for two and a half hour. Since the area of Si substrate which will be anodized is limited in size, to ensure an uninterrupted oxide growth aluminum is evaporated on its back surface before anodization. Al evaporation was done at a vacuum of less than 6.75×10^{-4} Pa. Windows of small dimension (1.5 by 0.5 mm square) were photolithographically constructed through the field oxide.

The electrolyte chosen was 0.04 M solution of KNO_3 in ethylene glycol. Fresh electrolyte was used for every anodization, since it is known that the aforementioned electrolyte is hygroscopic and water content in the electrolyte influences the oxidation[10]. No attempt was made in stop this absorption of water because it was assured by Revesz[11] that the effect of this absorption on the anodization efficiency is negligible. The anodization was performed

at room temperature. Current densities were varied from 3 to 30 mA/cm^2 during oxidation. Forming voltage of the anodization was usually terminated at 100 volt but except in one occasion where it was 60 volt. Current density was changed on the way of oxidation process to improve the electrical properties. The thickness of the oxide film was measured by using an ellipsometer. MOS structures were formed by evaporating 99.999 percent pure aluminum for the gate electrode with a diameter 400 μm.

Fugure 1 shows the fabrication steps of MOS capacitor with small-area anodic oxide. This device was used for evaluating the MOS C-V characteristics. The interface state density was measured by the Terman method[12], where the measurement frequency was 1 MHz and the applied gate voltage ranged from -25 to $+5$ volt.

The composition analysis of SiO_2/Si interface was done by X-ray photoelectron spectroscopy (XPS). The emission current and source power were 25 mA and 265 watt respectively. Experimental vacuum was maintained at the order of 10^{-10} Torr. XPS survey was carried out with voltage of electron multiplier set at 2300 V and with a pass energy of 100 eV. During multiplex, voltage of electron multiplier was adjusted at 2400 V and all multiplexed spectra were taken at a pass enegy 50 eV.

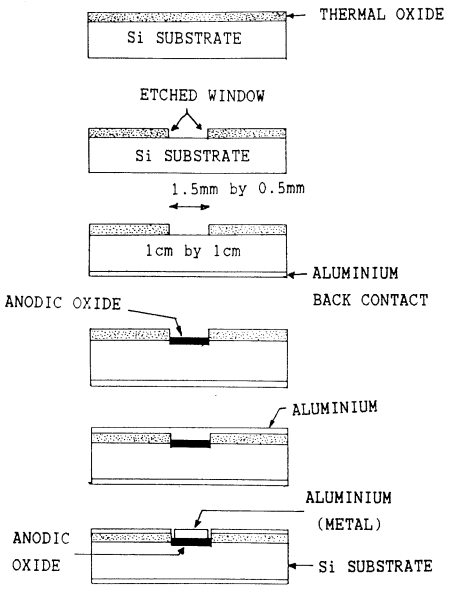

Figure 1 Fabrication step of a MOS capacitance.

3 RESULTS

3.1 V-t curve

The relation between cell voltage and oxidation time observed during the various anodization processes are shown in Figs. 2~4. Figure 2 shows two of the cases where constant current density was changed from 3 mA/cm^2 to 6 mA/cm^2 at forming voltages of 10 V and 20 V respectively and the oxidation was terminated at 100 V of forming voltage. The lower part of each curve is nonlinear up to certain point but beyond this, each attains linearity according to the relation

$$V(t) = rt + d_0 \qquad (1)$$

where d_0 is the initial cell voltage ; about 3 V in this case. The grown rate r, is a function of current density. V(t) is the forming voltage.

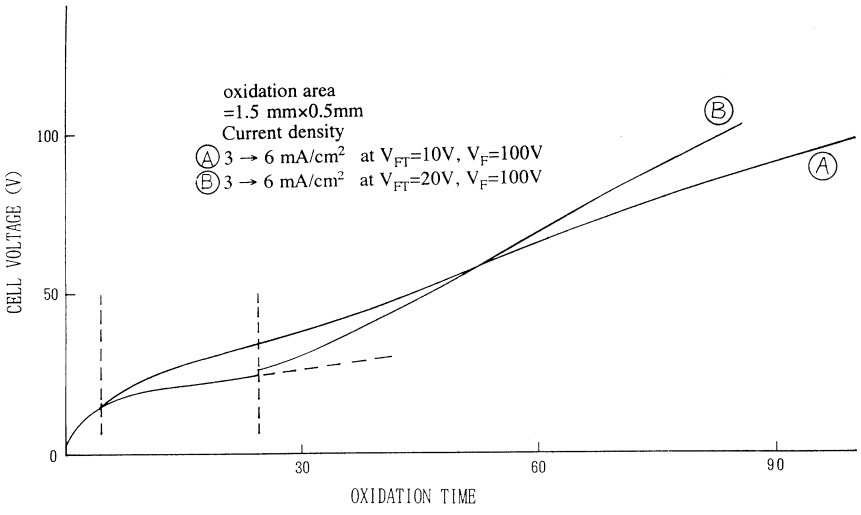

Figure 2 Cell voltage versus anodization time for two cases of small-area constant current anodization.

Next two cases are illustrated in Fig. 3. Where solid line was drawn for anodization carried out by a 6 mA/cm² current density and dashed line represents a multi-step constant current oxidation current density of which had gone through an arbitrary step-up transition. The step-down transition of current density was involved in a oxidation the cell voltage vs. time relation of which is represented in Fig. 4. In all the above five cases of oxide formation no considerable irregularities were found and the oxide grown can be regarded as steady and smooth.

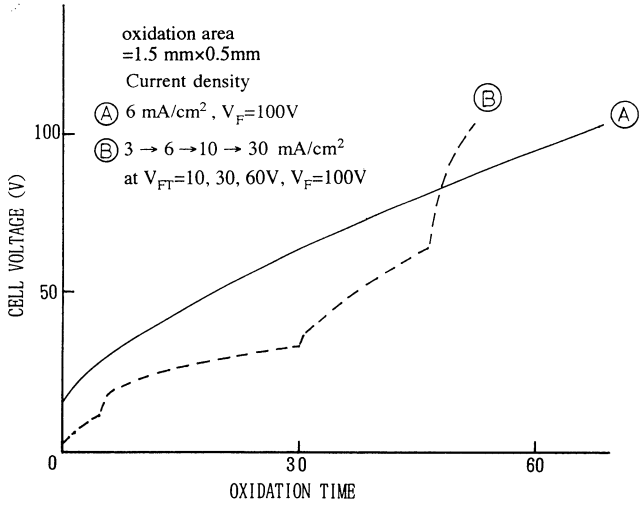

Figure 3 Cell voltage versus anodization time of the multi-step constant current anodization.

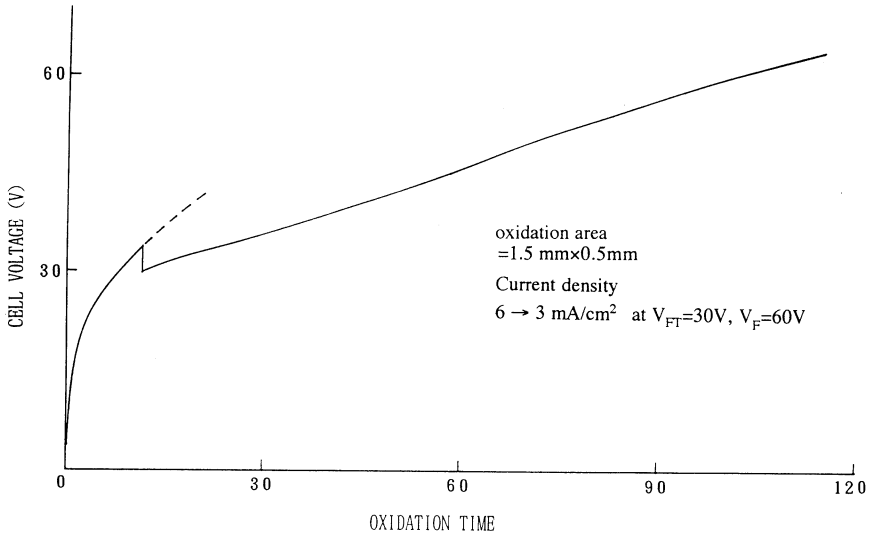

Figure 4 Cell voltage versus oxidation time of a constant anodization. Current density was stepped down during anodization.

3.2 Normalized Capacitance vs. Gate Bias

Three of the results are shown in Fig. 5 where ideal curve represents an $N_{it}=0$ situation. The experimental curve was found to have stretched out along the gate bias axis. Figure 5 illustrates the relation between normalized capacitance and gate bias for the case the current density of which was changed at three steps on the way to completing anodization. At every transition the current was adjusted to a higher value and is, therefore, termed as step-up transition. Figure 5 also exhibits the same relation for a sample which was anodized by a single step-down transition of current density. The symbol V_{FT} was used to denote the forming voltage at which the current density was altered. V_F is the final forming voltage. A comparison between step-up and step-down transition shows that experimental curve involving step-up transition ($3 \rightarrow 6 \rightarrow 10 \rightarrow 30$ mA/cm^2 at $V_{FT}=10$ V, 30 V and 60 V) was stretched more along the gate bias than that involving step-down transition ($6 \rightarrow 3$ mA/cm^2 at $V_{FT}=30$ V). The experimental curve approached to be an ideal one, i. e., the practical curve is less stretched after annealing treatment and this case is also shown in Fig. 5.

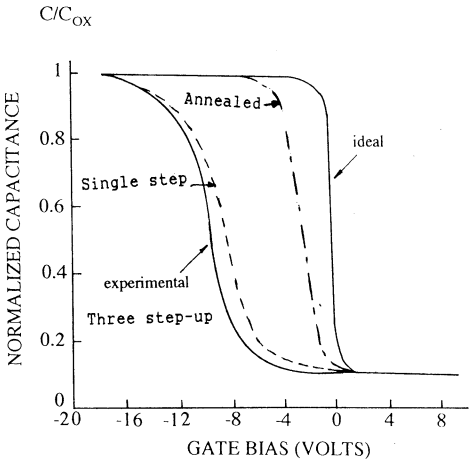

Figure 5 Capacitance stretch-out along the voltage axis due to interface trapped charges.

Surface-state density N_{it}, as a function of Si bandgap energy was calculated using the following relation[7]

$$N_{it}=C_{ox}/q[(d\Psi_s/dV_G)^{-1}-1]-C_S/q \quad cm^{-2}\,eV^{-1} \qquad (2)$$

where C_{ox} and C_S are oxide capacitance and silicon surface capacitance per unit area respectively, q is the electronic charge and $d\Psi_s/dV_G$ is the silicon band bending per unit of gate bias.

The surface state density along the band gap of silicon for a small-dimensional oxide is shown in Fig. 6. It was found that the surface state density decreases with increasing current density. This phenomenon is not in agreement with the N_{it} vs. energy relationship of a comparably large sized oxide because for the case of a large sized oxide, N_{it} decreases with decreasing current density[13]. For all samples, anodic oxidation area was same and had a value of 1.5 by 0.5 mm square, and each film was divided equally into three parts to get 0.4

by 0.4 mm square areas on which C-V measurement was made. Though the variation in the distribution of N_{it} over the silicon bandgap due to three different location of C-V measurement was almost negligible, curves having lowest midgap N_{it} were plotted in all cases for comparison. In all figures, V_{FT} denotes the forming voltage at the time of transition of current density.

From the results, shown in Fig. 7, it could be summarized that step-up transition of constant current density for small-dimension anodic oxide had some effect, though trivial, in minimizing the $Si-SiO_x$ interface traps. Although the anodization process which involved a $3 \rightarrow 10\ mA/cm^2$ intermediate transition of current density was effective in minimizing the midgap interface states considerably, it could not decrease interface states positioned near band edges. Figure 7 also includes the characteristics of the case in which the oxide film was grown via an intermediate step-down transition of current density.

Figure 8 illustrates the case where the anodization process, before completion, experienced three intermediate step-up transitions ($3 \rightarrow 6 \rightarrow 10 \rightarrow 30\ mA/cm^2$ at

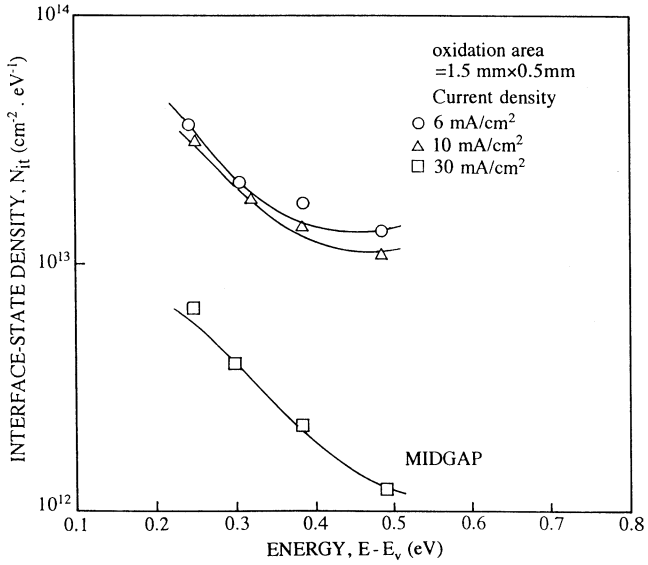

Figure 6 Distribution of interface states over the silicon bandgap in anodically oxidized silicon.

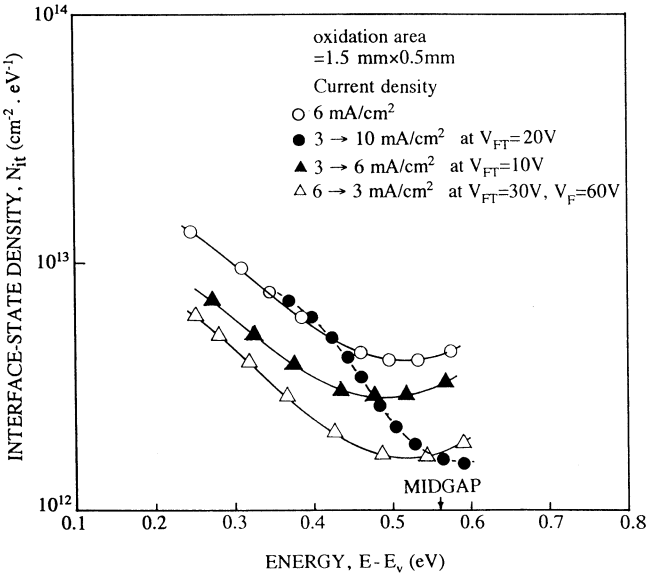

Figure 7 Change in the distribution of interface states over the silicon bandgap due to different cases in constant current anodization.

V_{FT}=10, 30 and 60 V). It is obvious from Fig. 8 that this case of multi-step transition of current density could not reduce interface states at all.

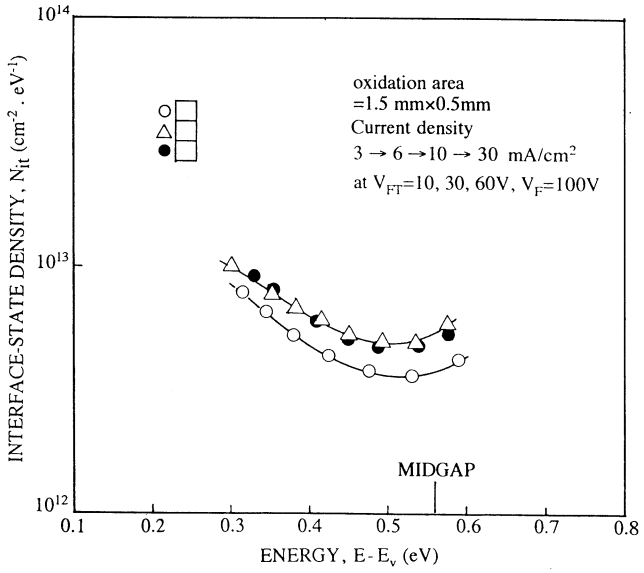

Figure 8 Variation in interface states with the location of C-V measurement.

Table I summarizes the midgap N_{it}s obtained for oxide samples formed by modified modes of constant current anodization, and this shows that single step-up or step-down transition of current density caused N_{it} to decrease. Midgap N_{it} can be considered as a representative value since the U-shaped curves appeared in Figs. 6, 7 and 8 vary smoothly throughout the bandgap. A comparison of bandgap interface-state density, for all the cases illustrated in Fig. 7, shows that the effect of step-down transition on the interface was superior than that of step-up transition in minimizing interface-state density.

Table I Midgap interface state density Nit for various modes of transition of current density.

current density mA/cm²	forming volt V_F, volt	midgap Nit ($cm^{-2}ev^{-1}$)	type of transition
6	100	4.2×10^{12}	no transition
3→6 at V_{FT}=10V	100	3.2×10^{12}	step-up(once)
3→10 at V_{FT}=20V	100	1.63×10^{12}	step-up(once)
3→6→10→30 at V_{FT}=10, 60, 60V	100	3.7×10^{12}	multi-step
6→3 at V_{FT}=30V	60	1.7×10^{12}	step-down(once)

So step-down transition is a case which requires critical interpretation. As it has already been mentioned that an intermediate step-up transition of 3 → 6 mA/cm² acted favorably to reduce interface states so it can be speculated that the transitions 6 → 10 mA/cm² and 10 → 30 mA/cm² had little effect on N_{it} or had acted detrimentally on the Si-SiO_x interface.

3.3 Composition of SiO_2/Si Interface

The O 1s spectra of 50 and 30 Å thick oxides are shown in Fig. 9 and Fig. 10. Each of these spectra was separated into two component spectra using least square method with the following assumptions: (1) each spectra comprises of two O 1s spectra, one of which is a contribution from SiO_2 and other one is from Cu_2O, (2) O 1s peak position of Cu_2O is at about 530.4 eV and that of SiO_2 is at about 533 eV[14]. O 1s peak appeared from thinner oxide was found to shift at a lower binding energy and this result is consistent with that of other researchers[15,16].

Si 2p spectra of 80 Å and 50 Å thick oxide are shown in Figs. 11 and 12. In both of these cases Si 2p signal of silicon bulk is almost absent but the spectra of 50 Å oxide showed a trace amount of Si 2p of silicon bulk. Si 2p spectra of the thinnest oxide appeared as shown in Fig. 13 where it was found that Si 2p of silicon bulk surpasses that of silicon oxide in intensity and prominence. Table II to V show different features associated with their corresponding spectra. Since analyzer pass energy was 50 eV, not 25 eV which is recommended for a good resolution spectra, resulting Si 2p spectra was far from having a standard shape.

This Si 2p spectra was compared with those of comparatively large-area oxide[16] to verify the degree of reliability of large-area etch rate which was used during etching of small-area oxide. The Si 2p spectra resulted from about 30 and 14 Å as-grown film of large-area anodic oxides are illustrated in Fig. 14 and 15. A comparison of these three illustrations elucidates that the actual thickness, remained after the etching of a small-area oxide, was less than that had been assumed. So Si 2p spectra in Fig. 13 could have appeared from a oxide film thinner than 30 Å. Though a poor S/N ratio did not allow an satisfactory separation of this spectra into its component, a somewhat separation was made to show that this spectra had contributions from intermediate oxides. In order to investigate the intermediate oxidation states, spectra in Fig. 13 are separated by the least square calculations in accordance with the following assumption: the intermediate oxidation states consist of three oxidation states, Si_2O, SiO, and Si_2O_3. Table VI contains relevant informations of the different intermediate oxides and shows per centages of contributions of the intermediate oxides which add up to give the total amount of silicon present in the remaining oxide film.

Si 2p spectra appeared from both small-dimension and large-dimension anodic oxide of about 30 Å had been separated into their components in accordance with the valence state of Si in the intermediate silicon oxide. The contribution from each of these Si atom in the

Table II. General features of the O ls spectra shown in Fig. 9.

Peak center eV	Height arb. unit	FWHM eV	Area %
533.647	2645	2.093	63.64
531.335	1562	2.081	36.36

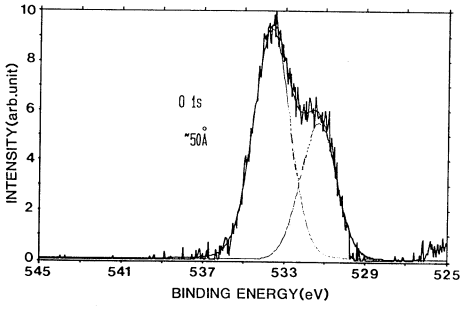

Figure 9 XPS Is spectra is separated into its component spectrum. Sample was small-area Si anodic oxide film.

Table III. General features of the O ls spectra shown in Fig. 10.

Peak center eV	Height arb. unit	FWHM eV	Area %
532.945	1892	2.3	68.71
531.12	1214	1.7	31.29

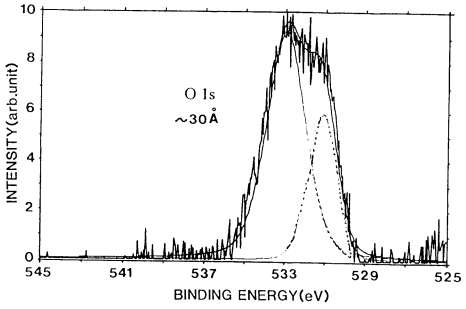

Figure 10 XPS O Is spectra of the 30ÅSi anodic oxide film.

Table IV. General features of the XPS Si 2p spectra shown in Fig. 11.

Charge up = 0.529eV		
Peak center eV	Height arb. unit	FWHM eV
104.006	1831	2.53

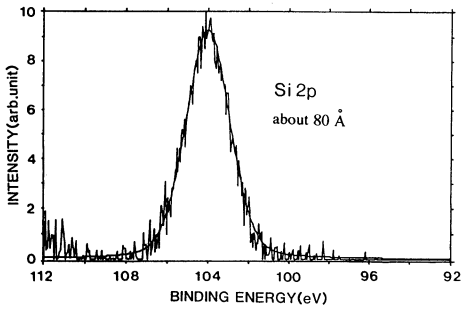

Figure 11 XPS Si 2p spectrum of the 80ÅSi anodic oxide film.

Table V. General features of the XPS Si 2p spectra shown in Fig. 12.

Peak center eV	Height arb. unit	FWHM eV
104.75	418	2.18

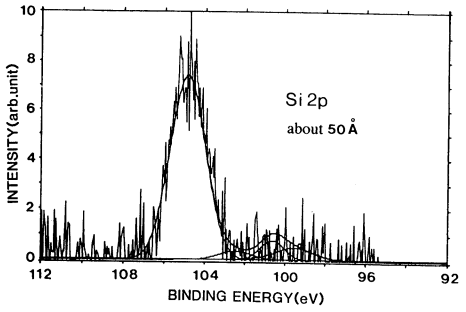

Figure 12 XPS Si 2p spectra of the 50ÅSi anodic oxide film.

Table VI. General features of different oxides obtained from separation of the XPS Si 2p spectra into its component.

Peak no.	Valence state	Peak center eV	Height arb. unit	FWHM eV	Area %
1	Si^{4+}	103.95	161	2.4	27.58
2	Si^{3+}	103.05	20	1.6	2.24
3	Si^{2+}	102.05	11	1..6	1.22
4	Si^{1+}	101.05	31	1.6	3.51
5	Si^{0}	99.75	575	1.6	65.45

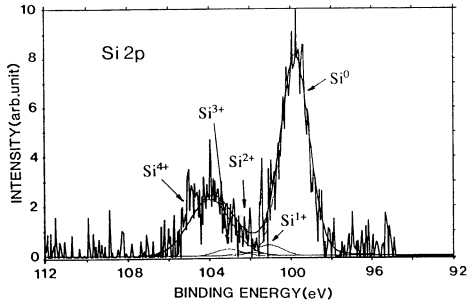

Figure 13 XPS Si 2p spectrum appeared form the 30 Å Small-area anodic oxide film.

Table VII. General features of the XPS spectra shown in Fig. 14.

Peak no.	Valence state	Peak center eV	Height arb. unit	FWHM eV	Area %
1	Si^{4+}	103.36	2198	1.88	40.47
2	Si^{3+}	102.32	502	1.39	6.84
3	Si^{2+}	101.16	245	1.26	3.04
4	Si^{1+}	100.14	190	1.34	2.48
5	Si^{0}	99.12	3764	1.28	47.17

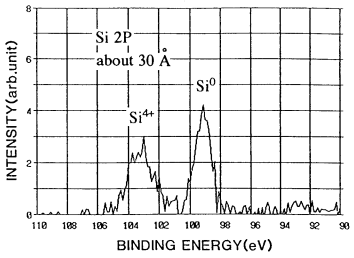

Figure 14 XPS Si 2p spectra of a comparatively large-area anodic oxide film[Ref. 28].

Table VIII. General features of the XPS skectra shown in Fig. 15.

	Peap center	Peak hight	FWHM	Area %
1	103.38 eV	1197.00	1.90	18.29
2	102.47	906.00	1.40	10.19
3	101.30	190.00	1.39	2.13
4	100.31	584.00	1.30	6.08
5	99.16	6299.00	1.25	63.31

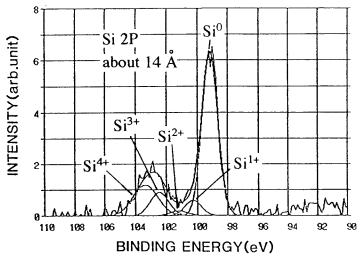

Figure 15 XPS Si 2p spectra of a comparatively large-area anodic oxidation film.

intermediate oxidation states in the composite Si 2p spectra, shown, in Fig. 14 and Fig. 15, are shown in Fig. 16 by bar diagram. It can be concluded that Si-SiO_2 interface of both small-area and large-area anodic oxide are non-stoichiometric in nature and it is Si rich.

4 DISCUSSION

There have been three speculative models proposed to explain interface trap level distribution in thermal oxide quantitatively : the coulombic[17], bond[18,19], and defect models. According to defect model, defects within or near the interfacial region may cause interface trap levels. This foregoing proposal has been made for Si thermal oxide and, therefore, could also stand valid for anodic oxide.

Three different types of defect that could exist at or near the Si-SiO_2 interface and might produce interface traps are (1) excess silicon[20] (trivalent silicon[21]), (2) excess oxygen[22] (nonbridging oxygen), and (3) impurities[23]. Recently Nanjo et al.[24] has analyzed anodic oxide film by XPS to study the chemical composition of the interface and they have suggested a silicon rich interface. Chemical bonds that compose the interface has been speculated[20] to have relation with the stoichiometry of the interface.

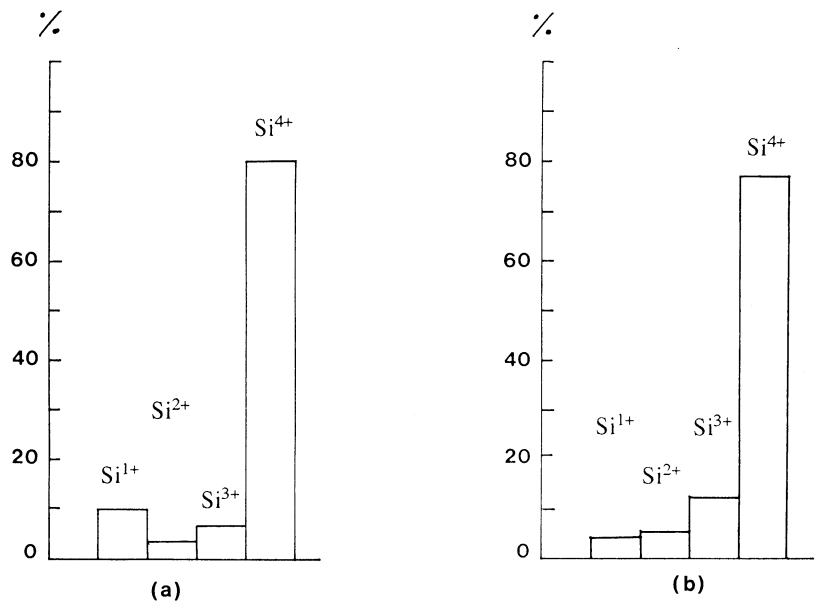

Figure 16 Si atoms having different valence states in the composition of Si-SiO_2 interface oxide of about 30 Å. (a) small-area anodic oxide, (b) large-area anodic oxide.

Anodic oxidation process for small-dimension Si might strongly affect the origins that are believed to induce interface states. Since all the sides of the small-dimdnsion film of anodic oxide layer were surrounded by thermal oxide, a distinct boundary between thermal oxide and anodic oxide could exist in a thermal oxide and anodic oxide. This difference in bond properties could create defects at the thermal-anodic oxide boundary and these defects in turn could cause a higher density of interface states at the thermal-anodic oxide boundary than that in the bulk of anodic oxide. It can be assumed that there could be two different mechanisms of anodic oxide formation in case of the small-dimension Si anodization: the first one of which could have dominated oxide formation at anodic-thermal oxide boundary according to the following relation as indicated in Fig. 16

$$V = f_1[J_{ib}(J,t),t] \tag{3}$$

where the forming voltage V is assumed to be dependent of time, t and Ionic current density at the boundary, J_{ib}. J_{ib} is assumed to be a function of time, even at a constant current density, J. Anodic oxide formation in the region other than boundary can be related to the equation

$$V = f_2[J_{io}(J,t),] \tag{4}$$

where J_{io}, the anodic current density in the bulk of oxide, as shown in Fig. 17, is also assumed to be a function of time and current density J. The formation of anodic oxide estimated by the forming voltage V was sure to have different growth rates for these two distinct regions, boundary and bulk, governed by equation 3 and 4 respectively. This difference in anodization process at boundary and in bulk of oxide during the same oxidation process could be responsible to cause the relationship between interface-state density and current density in case or a small -dimension anodic oxide to be reversed with respect to that of a comparatively large-dimension anodic oxide. It seems to be relevant here to mention that for the formation of large sized anodic oxide, ther-

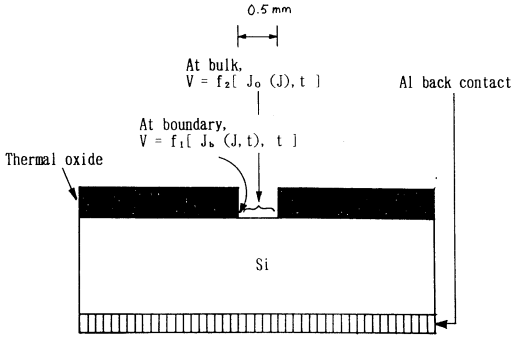

Figure 17 Proposed two regions governed by different anodic oxidation mechanism.

mal oxide is not required to form prior to the formation of anodic oxide.

The result that for small-dimension silicon oxide, interface-state density decreases with increasing current density could be interpreted by putting forward a suggestion that with a smaller current density, the leakage current results due to the defect at the thermal-anooic oxide boundary could cause a greater ratio of impurity/oxidation species through the silicon substrate other than boundary. These impurities, one of which could be potassium, present in the electrolyte used for anodization, would in turn induce interface states throughout the oxide interface. It was shown in Fig. 7 that step-up and step-down transition of current density during any oxidation process influenced the interface state density. Some plausible arguments in favor of the above results could be derived from the V-t curves, shown in Figs. 2 and 4, for three anodization processes. Each time a step-up or step-down transition had been brought about, the forming voltage built up across the oxide showed a sudden change of 2→5 volt in forming voltage just after the transition.

If ohmic law were satisfied, then for a constant conductivity, an increase in current density, J, from 3 to 6 mA/cm^2 could establish a forming voltage two times in value to that of before transition if the oxide thickness before the transition and just after the transition were same. The transition point voltage, however, was observed to experience a change less than 15%. There must be, therefore, some other factors which could affect conductivity of the anodic oxidation species through the already formed oxide at the transition point. Since the bond angle of silicon-oxygen is very soft and may be easily distorted at the interface[25], it is likely that these bonds could be affected by a change in electric field caused by the stepped transition of current density in an anodization process. The distortion or rearrangement of interface feature at any intermediate time during anodization could have left an interface which might have less traps than that in anodic oxide formed by a continuous anodization process.

In the case of a multi-step anodization, the stepped transition of current densities during oxide growth process could not decrease interface state density. In this case, it could be speculated that bond angles at the interface rearranged or distorted at the time of each 3→6 mA/cm^2, 6→10 mA/cm^2 and 10→30 mA/cm^2 transitions. These distortions would ultimately, when the anodization was finally terminated, have left an interface having enough trivalent Si-Si, often termed as dangling bond, stretched Si-Si bonds and stretched Si-O bonds to induce interface states of energies in the silicon band gap.

5 CONCLUSION

Interface states density, N_{it}, in a small-dimension film of silicon anodic oxide was found to have dependency on the current density of anodization process. N_{it}, for a given small-dimension oxide, 1.5 by 0.5 mm square in this study, showed a decrease with increasing current density. A considerable reduction in N_{it} occurred when, in these modified modes, the anodization process was made to go through a step-up or step-down transition before its completion. Among various transitions of current density, single step-down transition was found to have acted most favorably to decrease interface states. In this study, constant current mode was adopted during anodization keeping in mind that if the quality of oxide, formed by constant current mode had shown any improvement, its quality would certainly be improved if constant current mode were followed by constant voltage mode in the same oxide growth process. Small-dimension film of silicon oxide formed by a combination of modified constant current mode and constant voltage mode, if treated by low temperature annealing[26] would have interface-state density of the order 10^{10} which could be as effective as thermal oxide at least from the view point of interface states.

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